**Exp-2**

**BEGIN**

**1)**

**-Instantiate the Unit Under Test (UUT)**

**Uut: vlsi PORT MAP(**

**a=>a,**

**b=>b,**

**sel =>sel,**

**y=>y**

**);**

**2)**

Begin

A<”0101”;

B<=”0100”;

Sel<=”001”;

--hold reset state for 100 ns.

Wait for 100 ns;

a<”0101”;

b<=”0100”;

sel<=”010”;

--hold reset state for 100 ns

Wait for 100 ns;

a<=”0101”;

b<”0100”;

Sel<=”011”;

--hold reset state for 100 ns

Wait for 100 ns;

a<=”0101”;

b<”0100”;

Sel<=”101”;

--hold reset state for 100 ns

Wait for 100 ns;

a<=”0101”;

b<”0100”;

Sel<=”110”;

--hold reset state for 100 ns

Wait for 100 ns;

a<=”0101”;

b<”0100”;

Sel<=”111”;